Digital Video Interfacing Products

AT40USB

DVB-ASI input and output

Small Handheld size
No External Power Supply needed

Standard Features

- High Speed USB 2.0.
- Windows 2000, XP and **BDA / Direct Show** Drivers.
- Accompanied by DVSStaion2, Alitronika's Integrated TS Player, Recorder & Real Time Quick Analyser Software.
- Supports DVB Standards **A1010Rev1** and **EN50083.**
- Supports 188 /204 byte Packet Sizes.

Input
- Integrated Loop Through output.
- Carrier and Lock Detection.
- Sync, Error & Code Violation Detection.
- Automatic Cable Equalization of up to 350m.
- Support for Time Stamping, PID filtering.

Output
- Programmable Output Bit Rate.
- Null Packet Insertion by hardware.
- Selectable Burst size mode & continuous mode TS output.
- Hardware TS generation.

Application

Targeted for Digital Video Professionals, Sophisticated End Users and OEMs the AT40USB ***is an ideal solution for*** *A number of applications such as:*

- Development Tools.
- DVB to IP or IP to DVB Gateway.
- Transport Stream Recording.
- Transport Stream Playing.
- Transport Stream Analysing
- Transport Stream Monitoring.
- Video on Demand Server.
- Transport Stream Test Generator.
- High Speed Serial Data Link.
- PC TV using Alitronika's Direct Show compatible BDA Drivers.

Specifications

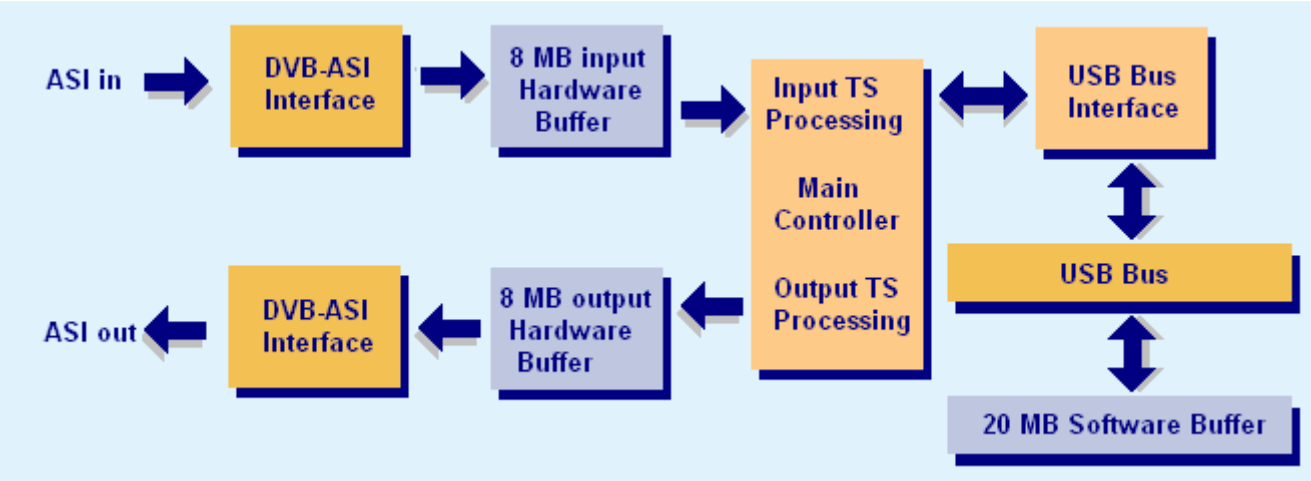
On Board Buffer: 8 Mbytes
Serial Connectors: 75 Ohms BNC
Input Return Loss: >15 dB
Input Signal level: 800 mV +/- 10%
Output Signal level: 1.0Vp-p nominal
DVB-ASI I/O Bit Rate: 0 to 214 Mbit/s
Bit Rate Stability: +/- 25ppm
DVB-ASI I/O Clock: 270 MHz
Size WxLxH: 120mmx100mmx30mm

1 GENERAL DESCRIPTION

A member of Alitronika's state of art digital video interfacing products.
The AT40USB is a USB based interface device suitable for Recording, Playing and Analyzing of DVB-ASI Transport Streams.

2 BLOCK DIAGRAM

FIG4 illustrates the block diagram of the AT40USB device. The device communicates with the PC via the USB interface device. On the input side, the serial data is de-serialized 8b/10b and de-coded before it is presented to PC via the USB controller device. On the output side, the MPEG-II transport streams enter the device via the USB interface device. The AT40USB then transmits the transport streams according to the settings provided by the application software. The data is 8b/10b encoded for DVB-ASI signals before it is serialized and transmitted via the BNC output connectors.



3 EXTERNAL INTERFACES

The external interfaces for the AT40USB are shown. There are two BNC connectors for the Serial input and output of DVB-ASI.
The three LEDs in front of the unit function as follows:

PWR - Top LED — Power LED
ON = Power is on
OFF = Power is off

CD - Middle LED — Play/ Record LED
ON = Device is Playing/Recording TS
Flashing = Play /Record not activated
In Record mode this LED indicates that a Carrier has been detected.
In Play mode this LED indicates that the output section has valid TS.

LCK - Bottom LED — LOCK LED
ON = Device is locked to TS
Flashing = No lock has been achieved
In Record mode this LED indicates that the device has locked into incoming TS.
In Play mode this LED indicates that the output section has locked into outgoing TS.

4 APPLICATION

Targeted for digital video professionals, sophisticated end users and OEMs the AT40USB is an ideal solution for a number of applications such as, development tools, universal interface for MPEG-II Transport Stream Playing and recording, video on demand server, transport stream test generator, high speed serial data link, software based MPEGII decoders & encoders and many other applications.

5 HARDWARE DESCRIPTION

5.1 USB interface device

The Cypress CY7C68013 High speed USB peripheral controller is for the USB interfacing. This device combines the USB 2.0 transceiver, SIE controller and a programmable peripheral interface in one chip.
Please refer to CY7C68013 Data book for more information about the operation and register setting of this device.

5.1.1 USB Interfacing

For the full description of USB Interfacing please refer to the Universal Serial Bus Interface Specification Revision 2.0 document. Alitronika Digital Interfacing Products comply with USB standard as defined by these specifications.

5.1.2 Data Transfer

The USB Specification document specifies that the USB transport data through a pipe between memory buffers associated with a software client on the host and an end point on the USB device. Data transported by message pipes is carried in the USB-defined structure. The USB provides different transfer types to match the requirement of the client software.

5.1.3 Control Transfers

Control transfers allow access to different parts of a device. They are intended to support configuration/command/status type communication flows between client software and its function. The USB device framework, Chapter 9, defines standards, device class, or vendor-specific requests that can be used to manipulate a device's state.

5.2 Main Controller

For the main controller the Altera Cyclone FPGA device is used. Most of the function of the AT40USB is carried out by the firmware residing in this device. The main controller configures and communicates with the various devices on board the AT40USB device. It carries out all the transport stream processing required by the application software, including data buffering, clock synthesizer, synchronization to the transport stream, time stamping, error flag generation, bit rate estimation and others.

5.3 Configuration Scheme

The FPGA on board most devices use SRAM configuration elements that require configuration data, better known as the firmware, to be loaded each time the device powers up. This process is called configuration. The description of configuration schemes used for such devices is beyond the scope of this document. A configuration device is almost always used. The devices are configured whenever the PC is powered up. Often this process is not carried out successfully and the device is not fully operational, the system must then be reset. Alitronika interface devices have provision for such a scheme, so it could be implemented on all the products if requested. But a much better scheme, whereby the configuration data is loaded by the application via the device driver is used. This gives Alitronika's products the flexibility that the firmware could be up-graded, customized and up-dated. More importantly, more than one firmware could be and has been developed for each device.
Instead of the FPGA being configured on power up, it could be configured at all times by the application, without the need for resetting the system. This method is called dynamic configuration scheme and places Alitronika's products at the top when it comes to flexibility and reliability.

6 THE INPUT

6.1 The Serial Input
The serial input section consists of mainly buffers, filters and the Cable equalizer device.

6.2 The Cable equalizer
The Gennum GS9064 Adaptive cable equalizer device is used to equalize and restore the input signal over 75Ohm co-axial cable optimized for performance at 270Mb/s. The cable equalizer section is designed to provide automatic cable equalization for cable length of up to 300 meters. Please refer to GS9064 data sheet, for more information about the operation this device.

6.3 Loop through serial output
A serial loop through output with integrated cable driver is provided for looping through the serial input during recording. The cable driver features an output mute on loss of signal, high impedance mode and adjustable signal swing. The output BNC connector is used for the loop through output during recording.

6.4 Input Transport stream processing
The Input data processing module, implemented in firmware, resides inside the main controller and carries out most of the input data processing. These include the following:

6.4.1 Packet size detection
The AT40USB can accept both 188 and 204 bytes packets. The 188 or 204 packet size flag is then set high accordingly.

6.4.2 Data Error Indication
Every byte of the transport packet which can not be decoded due to errors are indicated to the input transport stream processing unit. These errors are counted by a free running Data Error Counter and are presented to the application and are then displayed during recording and monitor modes. In addition a data error flag is raised when the number of errors are more than the number of acceptable errors for the integrity of the serial link to be maintained.

6.4.3 Sync Loss Error
The Packet Synchronizer Algorithm within the input transport stream processor, monitors the synchronization byte of the transport stream, H”47”, if it does not find it at the start of a packet, it indicates it to the application software in record and monitor modes by means of a Sync Loss Counter.

6.4.4 Input TS Bit Rate Estimation.
The input transport stream bit rate is obtained from the PCR. In cases such as RAW data mode the bit rate is estimated by counting the number of received packets in a certain time period and the calculating the bit rate.

6.4.5 Time Stamping
There are applications in which it is important to know the time of arrival of the transport packets. These applications include, real-time transport stream processing e.g. PCR correction, BRT (Bit Rate Trans-coding) and re-multiplexing of transport streams. The time of arrival of a transport packet is when the PCR byte, the 11th byte of the transport stream, enters the input data processing module.
The time stamp is derived from a 32bit reference clock counter running at the master clock frequency of the main controller.
On arrival of the 11th byte of the transport stream, the content of this counter is taken.
This 32bit time stamp value is then added to the end of the transport packet, hence creating a transport packet of 192 for a 188 byte packet or 208 byte for a 204 byte packet size.

6.4.6 PID Filtering
The AT40USB supports PID filtering. In order to avoid having long PID tables, two modes of PID filtering are used, Exclusive & Inclusive. In exclusive mode PIDs in the table are filtered out and in inclusive mode the PIDs in the table are kept and all other PIDs are removed.

6.4.7 RAW data mode
AT40USB can receive none DVB TS files of any kind to be played back. In this mode the AT40USB acts as fast serial data interface.

6.4.8 Data Buffering
It is beyond the scope of this document to explain the trivial details of streaming and buffering of the MPEG-II transport streams. It is sufficient to state that a DMA buffer is used to transfer data to the PC from the AT40USB device rather than direct read cycles. In addition to this software buffer, the AT40USB uses an 8Mbytes of SDRAM to implement a hardware input FIFO buffer. Two or three other internal FIFO’s are used by the main controller for smooth recording of the transport streams. In addition there are two 10Mb software buffers. The application software indicates the buffer usage during recording.

7 OUTPUT

7.1 The Serial Output
The serial output section consists of mainly buffers, filters and a line driver device.

7.2 Transmit FIFO Buffer
An 8Mbytes SDRAM is used to implement the transmit buffer. The buffer enables the AT40USB to generate low jitter DVB-ASI stream by compensating for any Bus latencies.
In addition to this rather large FIFO, two or three other internal FIFo's are used by the main controller for smooth transmission of the transport streams. There are also two 10Mb software buffers. The application software indicates the buffer usage during playing.

7.3 On board transmission clock and clock Synthesizer
An accurate 27MHz clock generator on board the AT40USB is used for the transmission of the output stream.
The byte rate clock of the transmitted transport stream is obtained from this clock using a clock synthesizer. Unlike other so-called "direct-digital synthesizers", the clock synthesizer on board AT40USB is not made up of a simple accumulator. It is based on a sophisticated algorithm to generate an accurate, jitter free output transmission even at high bit rates. The clock synthesizer obtains the transmission bit rate set by the application software, and generates a transmit pulse, which could be regarded as the byte rate for DVB-ASI transmission. One byte of the payload per transmit pulse is transmitted. In between these transmit pulses the controller transmits the stuffing character, K28.5 (Comma).

7.4 Transport packet size
AT40USB can transmit packet sizes of 188 or 204 bytes, in addition if desired it can generate a 204 byte transport packet from a 188 byte packet by adding 16 zero bytes to the end of the payload. This function is useful for the designers of receiver equipments to test if the system under development could handle both 188 and 204 packet sizes. The PCR is corrected by the application software accordingly.

7.5 Burst mode and Continuous mode
AT40USB can transmit transport stream in continuous mode in which the bytes are spread with stuffing " Comma" character filling the stream when there are no payloads. In the burst mode the transport packets are transmitted in user selectable burst sizes of up to the full packet size (188 or 204).

7.6 Null packet insertion by hardware
AT40USB allows the transmitted bit rate higher than of the bit rate of the transport stream file. In such cases the difference between the default bitrate and play bitrate is filled with Null packets. The PCR is corrected by the application software accordingly.

7.7 RAW data mode
AT40USB can play back none DVB TS files of any kind to be played back. In this mode the AT40USB acts as fast serial data interface.

Alitronika DVS
Operational register description

Version 3.102
Date: 20 June 2006

Lintdal36, 9725GD, Groningen, The Netherlands.

1 OPERATIONAL REGISTER

The operational registers of Alitronika's devices are listed below. Since all register accesses are 32 bit transfers, the operational registers are grouped into four 8-bit registers.

1.1 Record(input) Configuration Registers (read/write)

Record_Config Address = H"00"

Bit	Name	Function	level
0	DVB	Selects DVB Mode	High = Enabled
1	SMP	Selects SMPTE Mode	High = Enabled
2	RAW	Select Raw Mode	High = Enabled
3	RSV	Reserved (not use in current design)	Normally Low
4	LEN	Enable loop through output	High = Enabled
7:5	GRSET	Settings for GS9060 device	Set by software
8	ETS	Enable Time Stamping	High = Enabled
9	PID	Enable PID filtering	High = Enabled
10	TEX	PID Table Exclusive	High = Exclusive Table
12:11	RSV	Reserved (not use in current design)	Normally Low
14:13	ISEL [1:0]	Select input source	"0X": USB "10": SPI "11" : ASI/Tuner
15	PCLR	Clears PID table	High = Clear PID Table
16	RSPM	SPI input mode selection	0: Constant clock mode 1: Standard DVB-SPI mode
28:17	RSV	Reserved (not use in current design)	Normally Low
29	TRST	Tuner reset	High = Reset Tuner
30	RRST	Record reset, resets input modules	High = Reset
31	REN	Record Enable	High = Enabled

1.2 Play (Output) Configuration Registers (read/write)

Play_Config Address = H"04"

Bit	Name	Function	level
0	DVB	Select DVB Mode	High = Enabled
1	SMP	Select SMPTE Mode	High = Enabled
2	SER	Select Serial output	High = Enabled
3	PAR	Select Parallel output	High = Enabled
5:4	TPS[1:0]	Select TP packet Size	"00" = 188 "01" = 204 "10" & "11" = Reserved
6	PCREST	Rest amp PCR	High = Enabled
7	ADD16	Add 16 bytes to 188 TP	High = 188+16 Mode
8	RAW	Select Raw mode	High = Enabled
9	CLK27	Select 27MHz Clock for output	High =Clk27 Selected
10	EXCLK	Select External Clock for output	High = External clock
12:11	PSPM[1:0]	SPI output mode selection	Constant Clock or Standard
13	HTP	Enable hardware generated TS	High = Enabled
14	REMUX	Enable bitrate re-multiplexing	High = Enabled
15	CTP	Select if Null/Counter packets when BRREMUX or HTP is high	Low = Null packets High= Counter packets
18:16	GPSET	Settings for GS9062 device	Set by software
19	INV	Invert the ASI output signal	High = Enabled
29:20	RSV	Reserved (not use in current design)	Normally Low
30	PRST	Play reset, resets output modules.	High = reset
31	PEN	Play Enable	High = Enabled

1.3 Output file bitrate Registers (read/write)

Output file bitrate register Address = H"08"

Bit	Name	Function	level
31:0	OFBitRate	Bitrate of the file	

1.4 Output bitrate Registers (read/write)

Output bitrate register Address = H"0C"

Bit	Name	Function	level
31:0	OBitRate	Output Bitrate	

1.5 Output burst size Registers (read/write)

Output burst size Address = H"10"

Bit	Name	Function	level
31:0	Burstsize	Output Burst size	1 to188 or 1 to 204

1.6 Status& Error Registers (read only)

Status_Error Address = H"1C"

Bit	Name	Function	level
1:0	RTPS[1:0]	Input TP Size	"00"=188, "01"=204, "10" & "11" = Reserved
2	RSYNC	Synchronised to input data stream	High = In Sync
3	RCD	Carrier Detect	High = Carrier is detected
4	RLOCK	Locked to incoming transport stream	High = Locked
5	RCNTLK	Input bitrate is estimated.	High = Bitrate estimated
6	RPCRLK	Input bitrate is obtained from PCR.	High = Bitrate from PCR
7	RINV	Input DVB-ASI signal is inverted	High = Input is inverted
8	PLOCK	Locked to output stream	High = Locked
21:15	RSV	Reserved (not use in current design)	Normally low
22	RSDFE	Record SDRAM Fifo Empty	High = Fifo Empty
23	RSDFF	Record SDRAM Fifo Full	High = Fifo Full
29:24	RSV	Reserved (not use in current design)	Normally Low
30	PSDFE	Play SDRAM Fifo Empty	High = Fifo Empty
31	PSDFF	Play SDRAM Fifo Full	High = Fifo Full

1.7.1 Bitrate Byte count Registers (read only)

Bitrate Byte count Register Address = H"20"

Bit	Name	Function	level
31:0	BrBCnt	Bitrate data counter	

1.7.2 Bitrate Time interval Registers (read only)

Bitrate time interval Register Address = H"24"

Bit	Name	Function	level
31:0	BrTime	Bitrate time interval counter	

1.8 Data Error Registers (read only)

Data Error Registers Address = H"28"

Bit	Name	Function	level
31:0	Data Err	Data error counter	

1.9 Sync Error Registers (read Only)

Sync Error Registers Address = H"2C"

Bit	Name	Function	level
31:0	Sync Err	Sync error counter	

1.10 Hardware Buffers usage indicator Registers (read only)

Record SDRAM FIFO data count register Address = H"30"

Bit	Name	Function	level
31:0	RSRAM	Number of bytes in Record SDRAM fifo	

Play SDRAM FIFO data count register Address = H"34"

Bit	Name	Function	level
31:0	PSRAM	Number of bytes in Play SDRAM fifo	

1.11.1 PID table size Registers (read only)

PID Table Size Address = H"3C"

Bit	Name	Function	level
7:0	PID size	Size of PID table	Values: 1,2,4,8,16,32,64,128
15:8	Reserved	Reserved (not use in current design)	Normally Low
23:16	PID Wdused	Position of PIDs in PID table	0- PID table size

1.11.2 PID table Registers (read/write)

PID Table Address = H"60"

Bit	Name	Function	level
12:0	PID	PID number (read/write)	
13	PID valid	PID number valid (read)	High = Valid
31-14	Reserved	Reserved (not use in current design)	Normally Low

1.12 PCI access Registers (read/write)

Play_FIFO Address = H"80"

Bit	Name	Function	level
31:0	InData	Writes into on board FIFO	

Record_FIFO Address = H"80"

Bit	Name	Function	level
31:0	OutData	Reads from on board FIFO	

1.13.1 Tuner Data Write Registers (write only)

Tuner Data Write Address = H"90"

Bit	Name	Function	level
31:0	TWData	Tuner Write Data	Used by all devices

1.13.2 Tuner Communication Control Registers (read/write)

Tuner Communication Control Address = H"94"

Bit	Name	Function	level
7:0	TunerIdx	Command register Index	
11:8	DatabyteCnt[1:0]	Number of bytes for Read/Write	Used by all devices
12	R/W	Read/Write Action Indicator	1=Read 0=Write
15:13	TunerFunction	Device Select	"0"=PLL, "1"=Satellite, "2"=Cable, "3"=Terrestrial, "4"=Annex B0,"5"=Annex B1
31:16	RSV	Reserved	Normally Low

1.13.3 Tuner Communication Status Registers (read only)

Tuner Communication Status Address = H"98"

Bit	Name	Function	level
23:0	RSV	Reserved (not use in current design)	Normally Low
24	Busy	Communication in progress	HIGH=Busy
25	Slave Nack	Error on Slave communication	HIGH=Slave Error
26	Data Nack	Error on Data communication	HIGH=Data Error
31:27	RSV	Reserved (not use in current design)	Normally Low

1.13.4 Tuner Data Read Registers (read only)

Tuner Read Data Address = H"9C"

Bit	Name	Function	level
31:0	TRData	Tuner Read Data	

2 REGISTER DESCRIPTIONS

2.1 Record Configuration Registers

The record configuration registers apply to devices that support an input (recording).
The input source could be in any mode, DVB, SMPTE and RAW.

2.1.1 Record_Config Register1

RVS	RVS	RVS	LEN	RSV	RAW	SMP	DVB

Address: H"00"
Type: Write/Read
Reset: "00"
Description: This is the bits 0 to 7 of the record configuration register.

[0] DVB - Select DVB mode
Setting this bit high sets device into DVB mode.
[1] SMP - Select SMPTE mode
Setting this bit high sets device into SMPTE mode.
[2] RAW - Select RAW mode
Setting this bit high sets device into RAW mode.
[4] LEN – Enable Loop Through output
By setting this bit high loop through output is enabled.
[7:5,3] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.

2.1.2 Record_Config Register2

PCLR	ISEL1	ISEL0	RVS	RSV	TEX	PID	ETS

Address: H"01"
Type: Write/Read
Reset: "00"
Description: This is the bits 8 to 15 of the record configuration register.

[8] ETS - Enable Time Stamping
When set high the incoming transport streams are time stamped.
The time stamp is derived from the master clock. On arrival of the 11th byte of the transport stream, the PCR byte, the content of a 32bit free running counter is taken as the time stamp.
The 32bit time stamp value is then added to the end of the transport stream.
The application must be aware of the fact that the last four bytes of the transport streams are the time stamp value not pay load.
[9] PID - Enable PID filtering
Setting this bit high enables the PID filtering function.
[10] TEX – Exclusive or Inclusive PID table
In order to avoid having long PID tables, two modes of PID filtering are used.
When this bit is set high all the PIDs in the table are filtered out and when set low the PIDs in the table are kept and all other PIDs are removed.
[11:13] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[14:13] ISEL [1:0] - Input source select
These two bits form the input source select, "00" and "10" are used to indicate the device is a USB based devices and "10" selects the Parallel input and "11" the Serial input or the devices with tuners (DVB-T/S/C).
[15] PCLR – Clear PID Table
Setting this bit high clears the PID filtering table.

2.1.3 Record_Config Register3

RSV	RSV	RSV	RVS	RSV	RSV	RSV	PSPM

Address: H"02"
Type: Write/Read
Reset: "00"
Description: This is the bits 16 to 23 of the record configuration register.

[16] PSPM – Selects input mode of the DVB-SPI port
The DVB standard requires that DVB-SPI should have a clock that is 1/8th of the bitrate.
Often the TS source devices may use other formats. One commonly used format is a constant clock rate of 27Mhz with the "data valid" bit set high whenever there is valid data.
In such cases a so-called " Target adapter" is used.
Alitronika's devices allow for selection of this format for input without the need for such an adaptor.
When this bit is set low, the standard format is selected and when set high the constant clock rate format is selected for the parallel input.
[23:17] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.

2.1.4 Record_Config Register4

REN	RRST	TRST	RVS	RSV	RSV	RSV	RSV

Address: H"03"
Type: Write/Read
Reset: "00"
Description: This is the bits 24 to 31 of the record configuration register.

[28:24] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[29] TRST – Tuner Reset
Devices with tuner on board used this bit to reset the tuner settings whenever needed.
[30] RRST – Record Section Reset
This bit is used to reset all the input modules.
[31] REN - Record Enable
When set high the device starts recording transport streams.

2.2 Play Configuration Registers

The play configuration registers apply to devices that support an output (playing).
The output could be in any mode, DVB, SMPTE and RAW.

2.2.1 Play_Config Register1

Add16	PCREST	TPS1	TPS0	PAR	SER	SMP	DVB

Address: H"04"
Type: Write/Read
Reset: "00"
Description: This is the 8 LSB of the Play configuration register.
The Play configuration register holds all the values needed for correct setting of the hardware sources of output section.

[0] DVB - Select DVB mode
Setting this bit high sets device into DVB mode.
[1] SMP - Select SMPTE mode
Setting this bit high sets device into SMPTE mode.
[2] SER - Select Serial output
Setting this bit high selects the Serial output.
[3] PAR - Select Parallel output
Setting this bit high selects the Parallel output.
[5:4] TPS[1:0] - Transport Packet Size
These two bits select the transport stream packet size
"00" = 188 bytes "01" = 204 bytes
"10" & "11" = Reserved
[6] PCRST - Reset PCR enabled
This bit enables the application to reset the PCR
[7] ADD16 - Add 16 bytes to a 188 byte TS
This bit enables adding of 16 bytes to 188 byte TS to make 204 byte packet size.

2.2.2 Play_Config Register2

CTP	BRREMUX	HTP	PSPM1	PSPM0	EXCLK	CLK27	RAW

Address: H"05"
Type: Write/Read
Reset: "00"
Description: This is bits 8 to 15 of the Play Configuration Register.

[8] RAW- Select Raw data mode
Setting this bit high allows the device to play back none-DVB files.
[9] CLK27 - Select 27MHz clock
When set high the internal 27 MHz clock is selected for output data.
[10] EXCLK - Select External clock
When set high an external is selected for output data.
[12:11] PSPM[1:0] - Play SPI mode select
"00" = Constant clock mode for 188 packet size.
"01" = Standard DVB-SPI mode for 188 packet size.
"10" = Constant clock mode for 204 (including 188 + 16 byte) packet size.
"11" = Standard DVB-SPI mode for 204 (including 188 + 16 byte) packet size.
[13] HTP - Enable Hardware Generated TS
When set high the generation of TS by the hardware is enabled.
[14] BRREMUX - Enable Bitrate re-multiplexing
When this bit is high any output bit rate could be selected
[15] CTP - Select Null or Counter packets
When set low the hardware generates Null Packets & when set high Counter packet.

2.2.3 Play_Config Register3

RSV	RSV	RSV	RVS	INV	RSV	RSV	RSV

Address: H”06”
Type: Write/Read
Reset: “00”
Description: This is bits 16 to 23 of the Play Configuration Register.

[18:16, 23:20] RSV- Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[19] INV - Invert the output ASI signal
Setting this bit high inverts the DVB-ASI output signal a useful tool for testing DVB-ASI input devices for compatibility with DVB standards that require support for both true and inverted input ASI signals.

2.2.4 Play_Config Register4

PEN	PRST	RSV	RVS	RSV	RSV	RSV	RSV

Address: H”07”
Type: Write/Read
Reset: “00”
Description: This is bits 31 to 24 of the Play Configuration Register.

[29:24] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[30] PRST - Play Reset
When set high the play section modules are reset.
[31] PEN - Play Enable
When set high the device starts Playing transport streams.

2.2.5 Output File Bit Rate Register

OFBitRate[31:24]	OFBitRate[23:16]	OFBitRate[15:8]	OFBitRate[7:0]

Address: H”08”, H”09”, H”0A” and H”0B”
Type: Write/Read
Reset: “00”
Description: This 32 bit register contains the output file bit rate.
The bit rate of the file played is placed in this register. When the output source is not a TS file, the content this register must be set at maximum bit rate of 216000000.

2.2.6 Output Bit Rate Register

OBitRate[31:24]	OBitRate[23:16]	OBitRate[15:8]	OBitRate[7:0]

Address: H”0C”, H”0D”, H”0E” and H”0F”
Type: Write/Read
Reset: “00”
Description: This 32 bit register contains the output bit rate of the transport stream.

2.2.7 Output Burst size Register

RSV [31:24]	RSV [23:16]	RSV [15:8]	OBurstSize[7:0]

Address: H”10”, H”11”, H”12”, H”13”,
Type: Write/Read
Reset: “00”
Description: This register contains the output burst size of the transport stream.

[7:0] BurstSize[7:0] – Burst Size
[31:8] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.

2.3 Play & Record Error & Status Registers

Applicable to all devices.

2.3.1 Record_Status Register

RINV	RPCRLK	RCNTLK	RLOCK	RCD	RSYNC	RTPS1	RTPS0

Address: H"1C"
Type: Read
Reset: "00"
Description: This register contains the status of the input section.

[1:0] RTPS[1:0] - Received Transport Packet size
The packet size of the input transport stream is determined by the hardware synchronization mechanism. "00" indicated input transport packet size is 188 and when it is set "01" the input transport packet size is 204. Other conditions are currently not allowed
[2] RSYNC- Synchronised to input stream
When high it indicates the input is sync to incoming data.
[3] RCD - Carrier detect
This bit when high indicates a carrier signal is detected.
[4] RLOCK - Locked to input stream
This bit compliments bits 3 & 4 by indicating the input is now in lock & sync with the incoming data stream detected by the carrier detect.
[5] RCNTLK- Bitrate is estimated
The bit rate of the incoming Transport Stream is obtained from the PCR. In the absence of such a information (e.g. RAW data mode), the bit rate is calculated by the main controller.
[6] RPCRLK – Bitrate is obtained from PCR
This bit when set high indicated that the bit rate is obtained from the PCR.
[7] RINV- Input is Inverted DVB-ASI signal
When the input DVB-ASI signal is an inverted signal this bit is set high.

2.3.2 Play_Status Register

RSV	RSV	RSV	RSV	RSV	RSV	RSV	PLOCK

Address: H"1D"
Type: Read
Reset: 00
Description: This register contains the status of the output section.

[8] PLOCK – Play locked to the output TS
When the controller locks into the out going transport stream this bit is high to indicate that the output is in normal condition.
[15:9] RSV - Reserved
The reserved bits are either used by Alitronika's other devices or reserved for future development and are not used in the current version.

2.3.3 Record_Error Register

RSDFF	RSDFE	RSV	RSV	RSV	RSV	RSV	RSV

Address: H"1E"
Type: Read
Reset: "00"
Description: This register contains the error flags generated by the input section.
Since these bits are all error flags they are active high to indicate the error condition
[21:16] RSV - Reserved
The reserved bits are either used by Alitronika's other devices or reserved for future development and are not used in the current version.
[22] RSDFE - Record SDRAM Fifo Empty (underflow)
The SDRAM used as Fifo will set the PSDFE error flag HIGH whenever an underflow condition has occurred.
[23] RSDFF – Record SDRAM Fifo Full (overflow)
The SDRAM used as Fifo will set the PSDFF error flag HIGH whenever an overflow condition has occurred.

2.3.4 Play_Error Register

PSDFF	PSDFE	RSV	RSV	RSV	RSV	RSV	RSV

Address: H"1F"
Type: Read
Reset: "00"
Description: This register contains the error flags generated by the output section. Since these bits are all error flags they are active high to indicate the error condition.

[29:24] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[30] PSDFE - Play SDRAM Fifo Empty (underflow)
The SDRAM used as Fifo will set the PSDFE error flag HIGH whenever an underflow condition has occurred.
[31] PSDFF - Play SDRAM Fifo Full (overflow)
The SDRAM used as Fifo will set the PSDFF error flag HIGH whenever an overflow condition has occurred.

2.4 Record related Registers

Apply to all devices with support for input (s).

2.4.1 Bit Rate Byte Count Register

BrCnt[31:24]	BrCnt [23:16]	BrCnt [15:8]	BrCnt [7:0]

Address: H"20", H"21", H"22" and H"23"
Type: Read
Reset: "00"
Description: This 32 bit register contains the number of data bytes received during the time period contained in the " Time Interval " register.

2.4.2 Bit Rate Time Interval Register

BrTime[31:24]	BrTime [23:16]	BrTime [15:8]	BrTime [7:0]

Address: H"24", H"25", H"26" and H"27"
Type: Read
Reset: "00"
Description: This 32 bit register contains the time intervals during which the number of receive bytes are counted.
The bit rate of the incoming TS is normally obtained from the PCR. But there are cases that this information is not available in the PCR. In such cases the bit rate has to be estimated.
In order to be as accurate and at the same time as fast as possible to calculate the bit rate, a number of data byte is counted during a set period of time. This time interval is naturally shorter for the transport stream with higher bit rate.
The bite rate calculate using the following formula:
BitRate = (Clk Frequency / <BrTime>) * < BRCnt> *8

2.4.3 Input Data Error Register

DataErr[31:24]	DataErr[23:16]	DataErr[15:8]	DataErr[7:0]

Address: H"28", H"29", H"2A" and H"2B"
Type: Read
Reset: "00"
Description: This 32 bit register contains the number of data bytes errors.
Whenever the device detects an illegal code word during decoding of DVB-ASI transport stream, it generates a " Word Error " flag for the corresponding byte. A free running counter counts the number of errors. The Data Error Register contains the content of this error counter.
The Data error counter counts up for every error. There is no reset and the register may rap around. The application must compensate for these when this function is used to monitor data errors.

2.4.4 Input Sync Error Register

SyncErr[31:24]	SyncErr[23:16]	SyncErr[15:8]	SyncErr[7:0]

Address: H”2C”, H”2D”, H”2E” and H”2F”
Type: Read
Reset: “00”
Description: This 32 bit register contains the number of Sync Errors.
Whenever the synchroniser, which synchronises to the incoming DVB-ASI stream can not find the sync byte, H”47”, at the start of a transport packet, it increments a free running “ Sync Error”. The Sync Error Register contains the content of this counter. The Sync error counter counts up for every error. There is no reset and the register may rap around. The application must compensate for these when this function is used to monitor sync errors.

2.4.5 Record SDRAM FIFO data count Register

RSDRAM[31:24]	RSDRAM [23:16]	RSDRAM [15:8]	RSDRAM [7:0]

Address: H”30”, H”31”, H”32” and H”33”
Type: Read
Reset: “00”
Description: This 32 bit indicates the number of bytes in the 8 M Byte Record SDRAM.

2.5 Play related Registers

Apply to all devices with support for Output (s).

2.5.1 Play SDRAM FIFO data count Register

RSDRAM[31:24]	RSDRAM [23:16]	RSDRAM [15:8]	RSDRAM [7:0]

Address: H”34”, H”35”, H”36” and H”37”
Type: Read
Reset: “00”
Description: This 32 bit indicates the number of bytes in the 8 M Byte Record SDRAM.

2.6 PID Filtering Registers

Apply to all devices with support for input (s).

2.6.1 PID Table Size Register

RSV[31:24]	PIDPos[23:16]	RSV [15:8]	PIDSize [7:0]

Address: H”3C”, H”3D”, H”3E” and H”3F”
Type: Read
Reset: “00”
Description: This 32 bit indicates the number of bytes in the 8 M Byte Record SDRAM.

2.6.2 PID Table Register

RSV[31:24]	PIDPos[23:16]	RSV [15:8]	PIDSize [7:0]

Address: H”60”, H”61”, H”62” and H”63”
Type: Write/Read
Reset: “00”
Description: This 32 bit indicates the number of bytes in the 8 M Byte Record SDRAM.

The PID table is implemented by the Firmware of the main controller. The size of the PID table is represented in register H”3C”. The number of PIDs available in the table can also be read at address H”3C”. The PID table can be read/write sequentially. Bit 13 represents a valid PID during a read operation.
The PID filtering is controlled by 3 bits in the **Record Configuration register (H”00”).**
Bit 9 is the PID filtering enable register.
The PID table can only be accessed when this bit is low (PID filtering is disabled).
This is to stop changing the table while in use.
Bit 10 is the PID table exclusive bit. When this bit is high, all PIDs in the table are removed.
When the bit is low, the PIDs in the table are kept and all other PIDs are filtered out.
Bit 15 resets (clears) the PID table when set high.

2.7 PCI related Registers

Applicable to all PCI devices.

2.7.1 PCI Output Data Transfer Register

OutData [31:24]	OutData [23:16]	OutData [15:8]	OutData [7:0]

Address: H”80”, H”81”, H”82” and H”83”
Type: Write/Read
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & PCI device.

2.7.2 PCI Input Data Transfer Register

InData [31:24]	InData [23:16]	InData [15:8]	InData [7:0]

Address: H”80”, H”81”, H”82” and H”83”
Type: Write/Read
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & PCI device.

2.8 Tuner related Registers

Apply to all devices with support for Tuner input this include all DVB-T/S/C devices.

2.8.1 Tuner Data Write Register

TWData [31:24]	TWData [23:16]	TWData [15:8]	TWData [7:0]

Address: H”90”, H”91”, H”92” and H”93”
Type: Write
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & tuner.
This register is used by devices with tuners on board (DVB-T/S/C).

2.8.2 Tuner Communication Control Register

RSV [31:16]	Type[15:13]	R/W[12]	Data [11:9]	TunerIdex[7:0]

Address: H”94”, H”95”, H”96” and H”97”
Type: Write/Read
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & tuner.

[7:0] Tuner Index[7:0] – Command index number
[11:8] – Number of bytes in a read/write operation
A maximum of four bytes may be written or read by each operation.
[12] R/W – Read/Write operation indicator
A High indicates a read and a Low a write operation.
[15:13] Type[2:0] – Selects the Tuner Type
The NIM on board the DVB-T/S/C device is controlled by the main controller using an I2C bus. Each device has been allocated an address.

“0” = PLL device inside the tuner
“1” = DVB-S (Satellite)
“2” = DVB-C (Cable) Annex A
“3” = DVB-T (Terrestrial)
“4” = DVB-C (Cable) Annex B [0]
“5” = DVB-C (Cable) Annex B [1]

[31:16] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.

2.8.3 Tuner Communication Status Register

RSV [31:27]	Data Nack[26]	Slave Nack[25]	Busy[24]	RSV[23:0]

Address: H”98”, H”99”, H”9A” and H”9B”
Type: Write/Read
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & tuner.

[23:0] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version.
[24] Busy – Communication in progress
When high it indicates that the I2C bus is busy.
[25] Slave Nack – Error on Slave Communication
When high this bit indicates there is an error in communication between the NIM (tuner) device and the main controller on the I2C bus.
[25] Data Nack – Error on Data Communication
When high there is data communication error on the I2C bus.
[31:27] RSV - Reserved
The reserved bits are used by other Alitronika devices or are reserved for future developments and are not used in the current version

2.8.4 Tuner Data Read Register

TRData [31:24]	TRData [23:16]	TRData [15:8]	TRData [7:0]

Address: H”9C”, H”9D”, H”9E” and H”9F”
Type: Read
Reset: “00”
Description: A 32 bit register used for data transfer between main controller & tuner.

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